ABSTRACT OF THE DISCLOSURE

An exemplary skew-tolerant true-single-phase-clocking (TSPC) flip-flop is disclosed that reduces current spikes by allowing willful introduction of skew in the clock tree of a single-phase circuit design. More precisely, a split-clock TSPC flip-flop, which allows the flip-flop hold times to be met in the face of skewed clocks, which, in turn, reduces the maximum value of current spikes, can be substituted for a traditional TSPC flip-flop in a sequential logic circuit. The input of the split-clock TSPC flip-flop is latched according to a first clock signal, which was used in a preceding stage, while the output of the split-clock TSPC flip-flop is driven according to a second clock signal. The first and second clock signals can be skewed in time, but have the same frequency and substantially the same phase. Metal Oxide Semiconductor (MOS) device can also be included within the split-clock TSPC flip-flop to reduce power dissipation in cases of large clock skew.